

Power and the People

Real Designers and the State of the Art in Low Power Design

Buzz about low power and green engineering is everywhere. But what is the real state of the art in low power design, as reflected in today's design practices? Who cares about power? What power reduction techniques are most popular? When, and how, is power measured? When designers have power problems, clock-gating continues to be the first method in the arsenal that designers reach for. But voltage islands and powering down unused blocks are not far behind. The CPF and UPF low power standards have gained a lot of traction too, with over 80% of designers using one or both of these approaches to capturing power intent.

A survey of the current state of low power design was conducted by Envis Corporation in June 2008. The study comprised over 70 engineers and engineering managers from a variety of companies worldwide: IDMs, fabless, and design services companies.

Power is important across the full spectrum of semiconductor applications, which is no surprise. With consumer, portables and wireless early leading the drive for low power, servers, routers and other tethered devices are very sensitive to power / performance ratios and power density.

Consider the following:

- Chris Rowen of Tensilica found that electronics...accounted for 6% of electrical consumption, equivalent to thirty 800 MW power stations. (Ref. *Embedded Technology Journal*, July 8, 2008.)
- With the demand for computing power and the cost of electrical power continuing to escalate, power can be expected to consume a larger share of IT budgets, possibly as much as 50% in the next few years...According to HP, data center power densities have grown from 2.1 kWh/rack in 1992 to 14 kWh/rack in 2006. (Ref. *Force 10 Networks, Inc.: "Crisis in Power and Cooling"2007.*)

In the June survey, the respondents were roughly equal in four categories: consumer, multimedia, wireless and networking as shown below. About 60% of respondents were working in the US, and 27% in Japan.

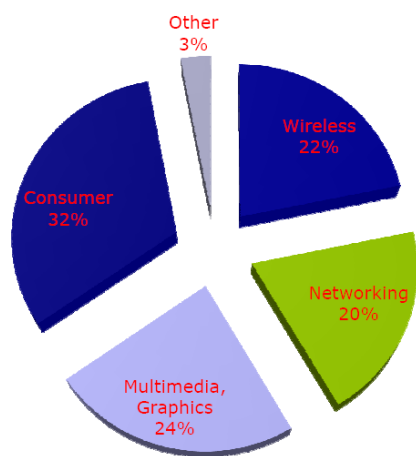


Figure 1: Application segments of respondents

Respondents' designs ranged from 100K gates to over 700M gates, with a frequency range of 20 MHz to 3 GHz centering around 500MHz.

Design and implementation teams ranged from designers who do 1 design per year, to those who do 50.

Design Parameter	Average of Responses
Design Size (M gates)	35
Frequency (MHz)	549
Number of SoC designs / year	15

Figure 2: Design parameters

It is interesting to note the current uptake of low power techniques in this snapshot; especially with regard to the emerging low power standards of the past 2 years enabling more sophisticated power management techniques. The breakdown is shown below, respondents indicating the techniques they are using today and expect to be using within one year.

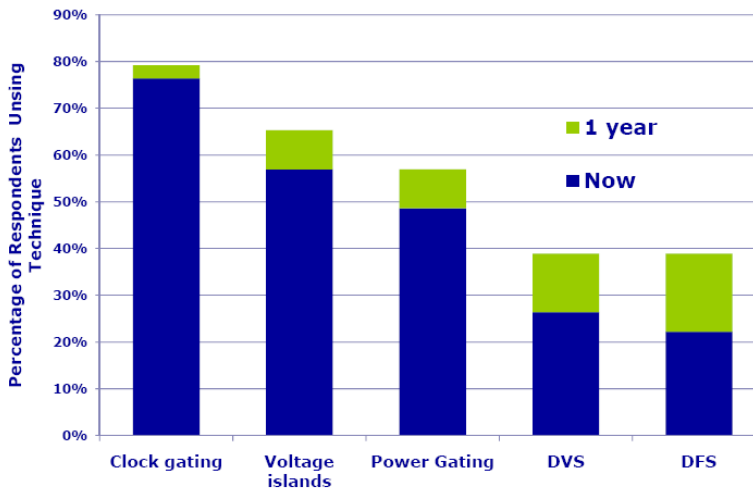


Figure 3: Uptake of low power techniques

So, what about the low power standards? In this survey, it emerges that 35% of the engineers are using both standards due to a mixed tool flow, with UPF in a total of 66% of the design environments (Synopsys, Magma, Mentor and Accellera Low Power) and 52% using CPF (Cadence and Si2 Low Power Coalition.)

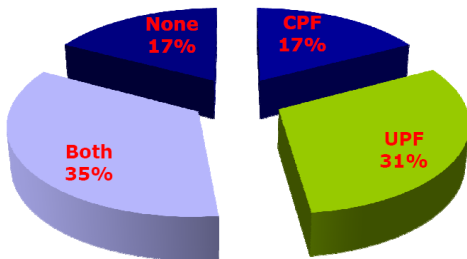


Figure 4: Adoption of low power standards

Taking a look at the steps in the design flow, over 60% of the respondents initially did a quick XL spreadsheet based on past experience. Over 35% estimated power at RTL, over 60% at the gate level before place and route, and 70% did an estimate for “power signoff” after place and route.

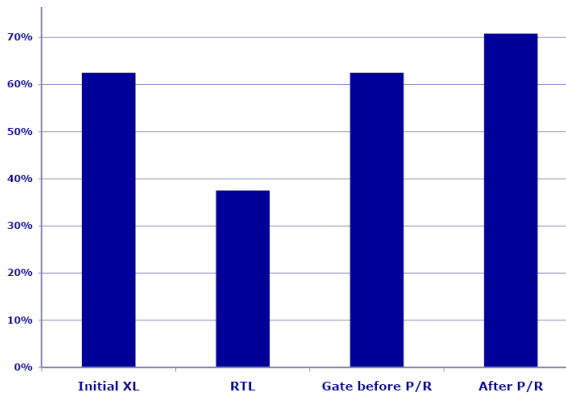


Figure 5: Where is power measured?

For power estimation, there is the challenge of determining stimulus that will provide a meaningful power estimation number. Based on responses, 55% use actual simulation vectors, 33% run “vectorless” modes of operation in power measurement tools, which generally do not provide very accurate results, and 12% highlighted the lack of meaningful vectors as a problem for them.

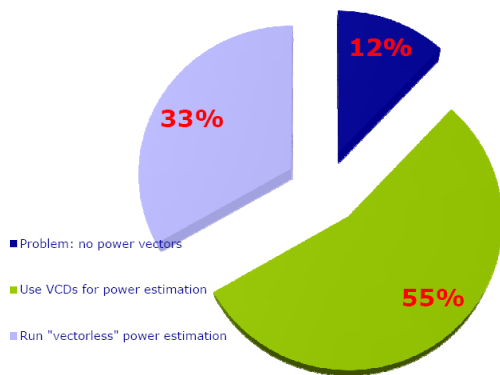


Figure 6: Stimulus for power measurement

Turning to design-specific information, it is no surprise that the most widely used IP was from ARM, who pioneered the Intelligent Energy Management, followed by Denali, Tensilica and MIPS.

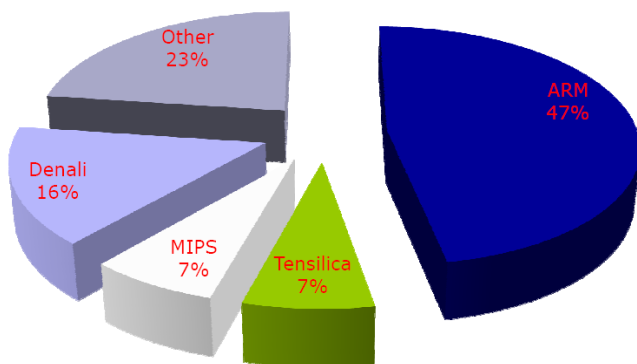


Figure 7: IP used in designs from survey

In this particular sampling, libraries ranged from TSMC (32%) to custom libraries (26%) to Artisan/ARM (14%) and Virage (8%). Over half of these engineers use .lib or .v libraries, with the more power-accurate CCS and ECSM trailing at 31% and 14% respectively.

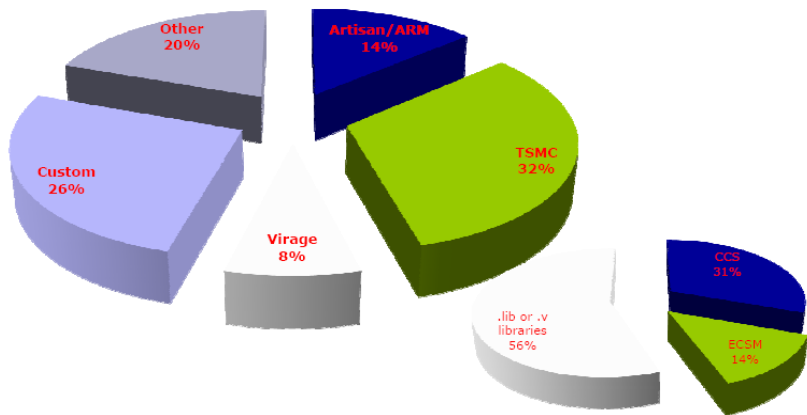


Figure 8: Libraries and library standards

The process node most SoCs are in right now is 65nm, but 45nm and below is where the acation is: by next year, designers say they will primarily be at 45nm.

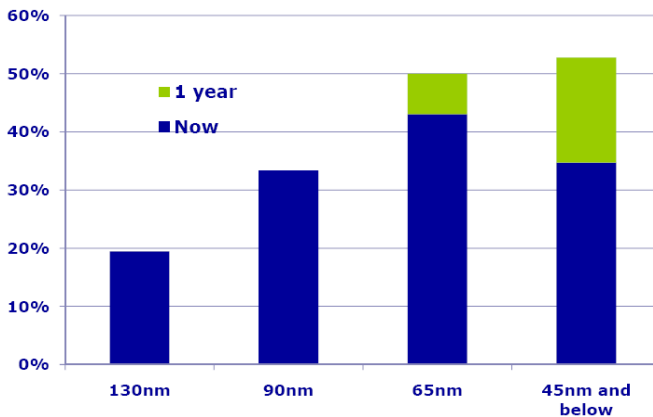


Figure 9: Process nodes

This survey shows a snapshot of the state of the art in low power designs and design practices today. As we move toward increasingly challenging low power goals for electronics, it will be interesting to continue to track these metrics and the evolution of low power design to chart a course toward best practices for all power-sensitive chips.

Holly Stump, VP Marketing, Envis Corporation.



4800 Patrick Henry Drive
 Santa Clara, CA 95054
 1.408.627.8252
www.envis.com